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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/724,193	12/01/2003	Stephen K. Sunter	LVPAT064US	1340

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EXAMINER	
LE, TOAN M	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 03/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/724,193	SUNTER, STEPHEN K.	
	Examiner	Art Unit	
	Toan M. Le	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,7 and 9-11* is/are rejected.

7)☒ Claim(s) *4,6 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-3, 5, 7, and 9-10 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 4, 2, 5, and 11 of copending Application No. 10/895,356.

A comparison in claims is presented in the table below:

Co-pending Application 10/895,356	Instant Application 10/724,193
1. A method of deducing properties of the shape of a waveform, the method comprising the steps of: (a) generating a signal based on a periodic pattern of logic levels; (b) measuring a DC level that is proportional to the average level of the signal and a DC level that is proportional to the average of the signal level squared; (c) calculating a property value of the shape of the waveform based on the plurality of measurements.	1. A method for deducing signal parameters of data signals, comprising: generating data signals that consist of predetermined data sequences; measuring average voltage of each said data signals; and deducing said parameters from said average voltages.
4. A method according to claim 1, said properties include one or more of the following properties: logic level voltage, logic level current, rise time, fall time, average transition time, pre-emphasis, duty cycle distortion.	2. A method as defined in claim 1, said parameters being logic voltages and rise and fall times.
2. A method according to claim 1, wherein said calculating a property value includes calculating the difference between two logic levels of the waveform, said periodic pattern of step (a) comprises a number of same logic values, and the periodic pattern of step (c) comprises a different number of same logic values.	3. A method as defined in claim 1, when said parameters are the difference between two logic levels, said measuring average voltages of each said data signals, including: (a) measuring average voltage for a periodic pattern containing a number of consecutive same-value logic values; (b) measuring average voltage for a pattern containing a different number of consecutive same-value logic values; and (c) performing a calculation based on measured average voltages to deduce the difference between two logic levels.
5. A method according to claim 1, wherein said calculating property value includes calculating effective rise and fall transition times, the periodic pattern of step (a) comprises a number of same logic values and the periodic pattern of step (c) comprises one or a combination of, a different number of same logic values, a number of consecutive same logic values; the same number of consecutive logic values but split into two or more groups of same consecutive logic values; and one or more isolated logic values surrounded by the opposite logic value.	5. A method as defined in claim 1, wherein when said parameters are the difference between effective rise and fall transition times, said measuring average voltages including: (a) measuring average voltage for a periodic pattern containing a number of consecutive same-value logic values; (b) measuring average voltage for a pattern in which the number of consecutive same-value logic values are split in two or more groups of same-value logic values; and (c) performing a calculation based on measured average voltages to obtain the difference between effective rise and fall transition times.
5. A method according to claim 1, wherein said calculating property value includes calculating effective rise and fall transition times, the periodic pattern of step (a) comprises a number of same logic values and the periodic pattern of step (c) comprises one or a combination of, a different number of same logic values, a number of consecutive same logic values; the same number of consecutive logic values but split into two or more groups of same consecutive logic values; and one or more isolated logic values surrounded by the opposite logic value.	7. A method as defined in claim 1, wherein when said parameters are rise and fall transition times, said measuring average voltages including: (a) measuring average voltage for a periodic pattern containing a number of consecutive same-value logic values; (b) measuring average voltage for a pattern containing a different number of consecutive same value logic values; (c) measuring average voltage for a pattern in which said number of consecutive same-value logic values is split into two or more groups of same-value logic values; (d) measuring average voltage for a pattern containing one or more isolated logic values surrounded by the opposite logic value; and (e) performing a calculation based on measured average voltages to obtain rise and fall transition times.
11. A method according to claim 1, further including using said method to test a circuit and including a step of comparing the calculated value to a test limit to determine whether the circuit passes or fails the test.	9. A method of testing a digital circuit, comprising deducing parameters as defined in claim 1 and comparing deduced parameter values against expected parameter values to determine whether said digital circuit passes or fails.
11. A method according to claim 1, further including using said method to test a circuit and including a step of comparing the calculated value to a test limit to determine whether the circuit passes or fails the test.	10. A method of testing an analog circuit, comprising deducing parameters as defined in claim 1 and comparing deduced parameter values against expected parameter values to determine whether said analog circuit passes or fails.

Although the conflicting claims are not identical, they are not patentably distinct from each other because the scope in claims 1-3, 5, 7, and 9-10 of application's is equivalent in scope to claims 1, 4, 2, 5, and 11 of the co-pending application's.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Allowable Subject Matter

Claims 4, 6, and 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The reason for allowance of the claims 4, 6, and 8 is the inclusion of performing calculation before and after performing step (b), which is measuring average voltage for a pattern containing a different number of consecutive same-value logic values and comparing the average voltage measured in step (b) to an expected average voltage that would produce an acceptable difference between the two logic levels.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-2 and 9-11 are rejected under 35 U.S.C. 102(a) as being anticipated by "Evaluation Method of the Average Pulse Amplitude in a High-Speed Signal Integrity test System", Nastase et al. (referred hereafter Nastase et al.).

Referring to claim 1, Nastase et al. disclose a method for deducing signal parameters of data signals (Abstract), comprising:

generating data signals that consist of predetermined data sequences (Page 523, section I. Introduction and section II. Definition of the Average Pulse Amplitude);

measuring average voltage of each data signals (pages 523-525, section IV. Method Description); and

deducing the parameters from the average voltages (pages 523-525, section IV. Method Description).

As to claim 2, Nastase et al. disclose a method for deducing signal parameters of data signals (Abstract), said parameters being logic voltages and rise and fall times (page 525, section V. Simulation; figures 3-6).

Referring to claims 9-10, Nastase et al. disclose a method for deducing signal parameters of data signals (Abstract), comprising comparing deduced parameter values against expected parameter values to determine whether the digital circuit/analog circuit passes or fails (page 524, 2nd col., 1st, 2nd, and 3rd paragraphs to page 525, 1st and 2nd col.).

As to claim 11, Nastase et al. disclose a method for deducing signal parameters of data signals (Abstract), further including:

comparing deduced logic voltages and rise and fall times values of a circuit output signal to deduced logic voltages and rise and fall times of a circuit input signal to determine circuit gain or frequency response (figure 7).

Response to Arguments

Applicant's arguments with respect to claims 1-11 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toan M. Le whose telephone number is (571) 272-2276. The examiner can normally be reached on Monday through Friday from 9:00 A.M. to 5:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571) 272-2269. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Toan Le

February 27, 2006

MICHAEL NGHIEM
PRIMARY EXAMINER